GPIB-VXI/C

User Manual

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With compliments

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Chapter 1
General Description

This chapter contains a brief overview of the GPIB-VXI/C and its VXIbus and GPIB capabilities. This chapter also contains an overview of the local command set, an introduction to Code Instruments (CIs), and a description of the front panel.

Overview

The GPIB-VXI/C is a C-sized VXIbus module that links the industry standard IEEE-488 (GPIB) bus and the VXIbus. The GPIB-VXI/C performs transparent conversion of the GPIB signals and protocols to VXIbus signals and protocols, so that a GPIB Controller can control VXIbus instruments in the same way that it controls GPIB instruments. Figure 1-1 shows the GPIB-VXI/C interface module.

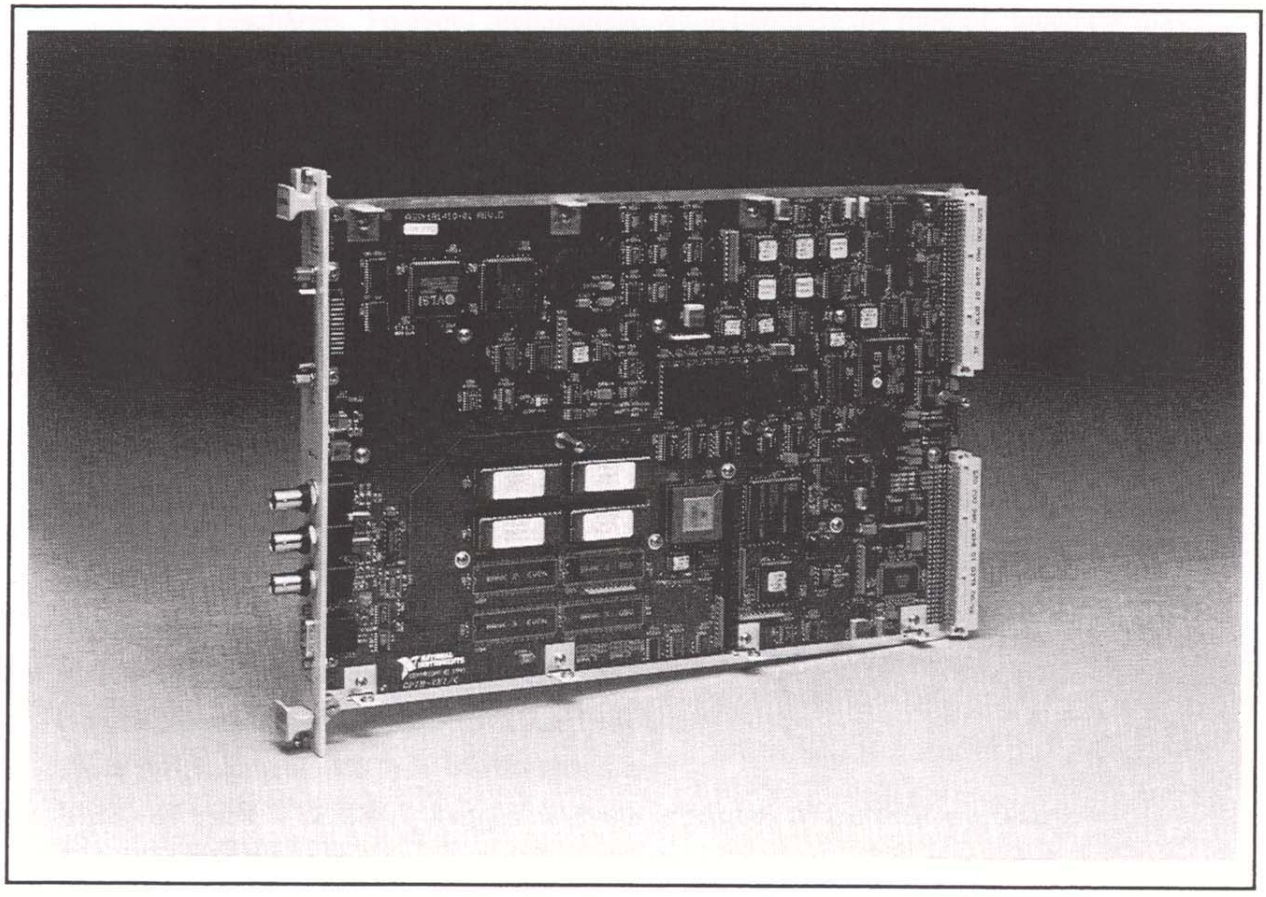

Figure 1-1. The GPIB-VXI/C Interface Module

The GPIB-VXI/C is factory configured to function as the system Resource Manager (RM). It performs the VXIbus startup configuration, self-test, and initialization functions, as well as VXIbus Slot 0-related services.

The RM and Slot 0 functions can be defeated individually so that the GPIB-VXI/C can coexist with another RM and/or be located in any slot.

What Your Kit Should Contain

Your GPIB-VXI/C kit contains a GPIB-VXI/C module and documentation. The GPIB-VXI/C part number and serial number are printed on the label affixed to its shield casing.

Note: The full part number of the GPIB-VXI/C is determined by configuration options corresponding to the extension *-XYZM* in the part number. The *X*, *Y*, and *Z* options are described below. The *M* corresponds to the manufacturer.

X	68881 coprocessor option	
	0	without coprocessor
	1	with coprocessor
Y	ROM option	
	1	user firmware
	2	development firmware
	3	user firmware and EPROM expansion
	4	development firmware and EPROM expansion
Z	RAM option	
	1	512 KB
	2	1 MB
	3	2 MB
	4	4 MB

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Optional Equipment

You can contact National Instruments to order any of the following cables.

- Type S5 serial port cable, 25-pin (2 m)
- Type S6 serial port cable, 9-pin (2 m)
- Type X2 double-shielded GPIB cables (1 m, 2 m, 4 m, or 8 m)

Unpacking

Follow these steps when unpacking your GPIB-VXI/C:

1. Verify that the pieces contained in the package you received match the kit parts list. Do not remove the module from its plastic bag at this point.
2. Your GPIB-VXI/C module is shipped packaged in an antistatic plastic bag to prevent electrostatic damage to the module. Several components on the module can be damaged by electrostatic discharge. To avoid such damage while handling the module, touch the plastic bag to a metal part of your VXIbus mainframe chassis before removing the module from the bag.
3. Remove the module from the bag and inspect the module for loose components or any other sign of damage. Notify National Instruments if the module appears damaged in any way. *Do not* install a damaged module into your VXIbus mainframe.

VXIbus Characteristics

The GPIB-VXI/C has the following VXIbus capabilities:

- Fully compatible with VXIbus System Specification
- VXIbus Resource Manager (RM) (defeatable)
- VXIbus Slot 0 support (defeatable)
- VXIbus Message-Based Commander and Message-Based Servant
- VXIbus master (A16, A24, D16, D08(EO))
- VXIbus slave (A16, A24, A32, D16, D08(EO))
- Up to 4 Megabytes of dual-ported (shared) memory
- Three programmable VXIbus interrupt handlers
- IEEE 488.1 and IEEE 488.2-compatible multiple primary or multiple secondary 488-VXIbus translator

GPIB Characteristics

The GPIB-VXI/C has the following GPIB characteristics:

- Communication with VXIbus Message-Based devices
  - VXI logical addresses are mapped to GPIB addresses
  - Automatically configured at startup
  - Programmable
- Interface
  - NAT4882 and Turbo488 ASICs coupled with DMA
  - Full, transparent support of individual status bytes for each GPIB address
  - Buffered operation decouples GPIB and VXIbus operation
  - Controller can address one VXIbus device to talk and one or more other VXIbus devices to listen
- IEEE 488.1 capabilities
  - SH1 (Source Handshake)
  - AH1 (Acceptor Handshake)
  - T5, TE5 (Talker, Extended Talker): multiple primary or multiple secondary addressing
  - L3, LE3 (Listener, Extended Listener): multiple primary or multiple secondary addressing
  - SR1 (Service Request)
  - DC1 (Device Clear)
  - DT1 (Device Trigger)
  - RL0 (Remote Local)
  - PP0 (Parallel Poll)
- IEEE 488.2-compatible 488-VXIbus translation

The IEEE 488.1 capabilities are supported for all VXIbus devices associated with GPIB addresses. The IEEE 488.2 compatibility applies to 488.2-compatible VXIbus devices associated with GPIB addresses through the GPIB-VXI/C.

Local Command Set Overview

The GPIB-VXI/C local command set supports the following types of operations:

- System configuration and control
  - Help
  - General configuration
  - RM information extraction
  - VXI-defined common ASCII system commands
  - Dynamic system configuration and reconfiguration
  - GPIB address configuration
  - VXIbus interrupt handler configuration
  - IEEE 488.2 common commands
- Instrument development and test
  - VXIbus access
  - Word Serial communication
- CI use and development
  - CI configuration

You can access the command set from the GPIB port, the serial port, and through Word Serial Protocol communication. You can also use separate programmable local command response modes for interactive and control program operation.

Code Instruments

The GPIB-VXI/C can run software modules called *Code Instruments* or *CIs* that perform special functions in the VXIbus environment. Typical applications of CIs include:

- Translating and interpreting command language
- Creating virtual (hierarchical) instrument
- Implementing Message-Based interface for Register-Based devices and non-VXI devices

CIs can be implemented in three forms:

- As part of the National Instruments-supplied firmware (*Resident CIs*, or *RCIs*)
- As user-developed downloadable object code (*Downloaded CIs*, or *DCIs*)
- As user-add-on firmware (*EPROMed CIs*, or *ECIs*)

For more information about CI capabilities and applications, see Appendix A, *Code Instrument Overview*.

Front Panel Features

The GPIB-VXI/C has the following front panel features:

- Five front panel LEDs
  - *SYSFAIL* LED reflects the status of the backplane SYSFAIL* signal and indicates that a VXIbus device in the system has failed.
  - *FAILED*, *TEST*, and *ON LINE* LEDs indicate the current status of the GPIB-VXI/C.
  - *ACCESS* LED indicates when the GPIB-VXI/C is accessed from GPIB or VXIbus or when its MODID is asserted.
- Five front panel connectors
  - GPIB interface
  - Serial port
  - Trigger input
  - Trigger output
  - External CLK10 I/O
- Configurable reset pushbutton
  - Pushbutton resets backplane
  - Pushbutton resets GPIB-VXI/C
  - Pushbutton resets both backplane and GPIB-VXI/C

Chapter 2
Configuration and Startup Procedures

This chapter contains information about the system configuration, GPIB-VXI/C configuration, and startup operation.

System Configuration

The typical system includes the following components:

- A VXIbus system mainframe containing the GPIB-VXI/C and instrument modules
- A host computer with a GPIB interface module and associated driver software (available for many computers from National Instruments) connected to the GPIB-VXI/C GPIB port
- A dumb terminal or host running a terminal emulator connected to the GPIB-VXI/C serial port (optional)

The serial port settings are 9600 baud, 8-bit data, no parity, and one stop bit. Refer to Appendix D, *Connectors*, for descriptions of the RS-232 serial connector and the GPIB interface connector.

Cables for connecting the GPIB-VXI/C serial port to an RS-232 terminal or COM1 port on an IBM PC-compatible computer are available from National Instruments (see *Optional Equipment* in Chapter 1).

GPIB-VXI/C Configuration

The GPIB-VXI/C factory configuration is shown in Table 2-1. The RAM, firmware and coprocessor are configured according to the GPIB-VXI/C purchase options.

Table 2-1. GPIB-VXI/C Factory Configuration

Function	Factory Configuration
Startup Mode	488-VXI Runtime System Mode
VXIbus Characteristics Resource Manager (RM) Logical Address Servant Area Size Shared Memory Address Modifiers	 Enabled 0 0 0% of Installed Memory Supervisor A16, Supervisor A24 data
VXIbus Slot 0 Services CLK10 Driver CLK10 Source SYSCLK Driver Priority Arbiter Bus Timeout	 Enabled Onboard Clock Enabled Enabled Enabled (BTO ≥ 250 µsec)
Bus Requester	Level 3
VXI Interrupt Handlers	Unassigned
GPIB Addressing Mode	Multiple Secondary Addressing
GPIB-VXI/C GPIB Primary Address	1
Serial Port System Startup Messages Console Local Command Port Discrete Fault Indicator (DFI)	 Disabled Enabled Normally Open
Front Panel BNC Termination External Clock Input External Trigger Input	 Unterminated Unterminated

You do not have to change the GPIB-VXI/C factory configuration to use it as a Slot 0 Resource Manager. The following pages describe the factory configuration settings and present alternate configurations.

Figure 2-1 shows the location of the GPIB-VXI/C configurable components and their physical location relative to some of the major circuit components. The jumpers and switches are represented in their factory default positions.

Note: The GPIB-VXI/C is housed in a metal enclosure that has cut-outs for access to all switches and jumpers associated with Slot 0/Non-Slot 0 settings, start-up mode, and Shared RAM settings. Under normal circumstances, you should not find it necessary to open the enclosure.

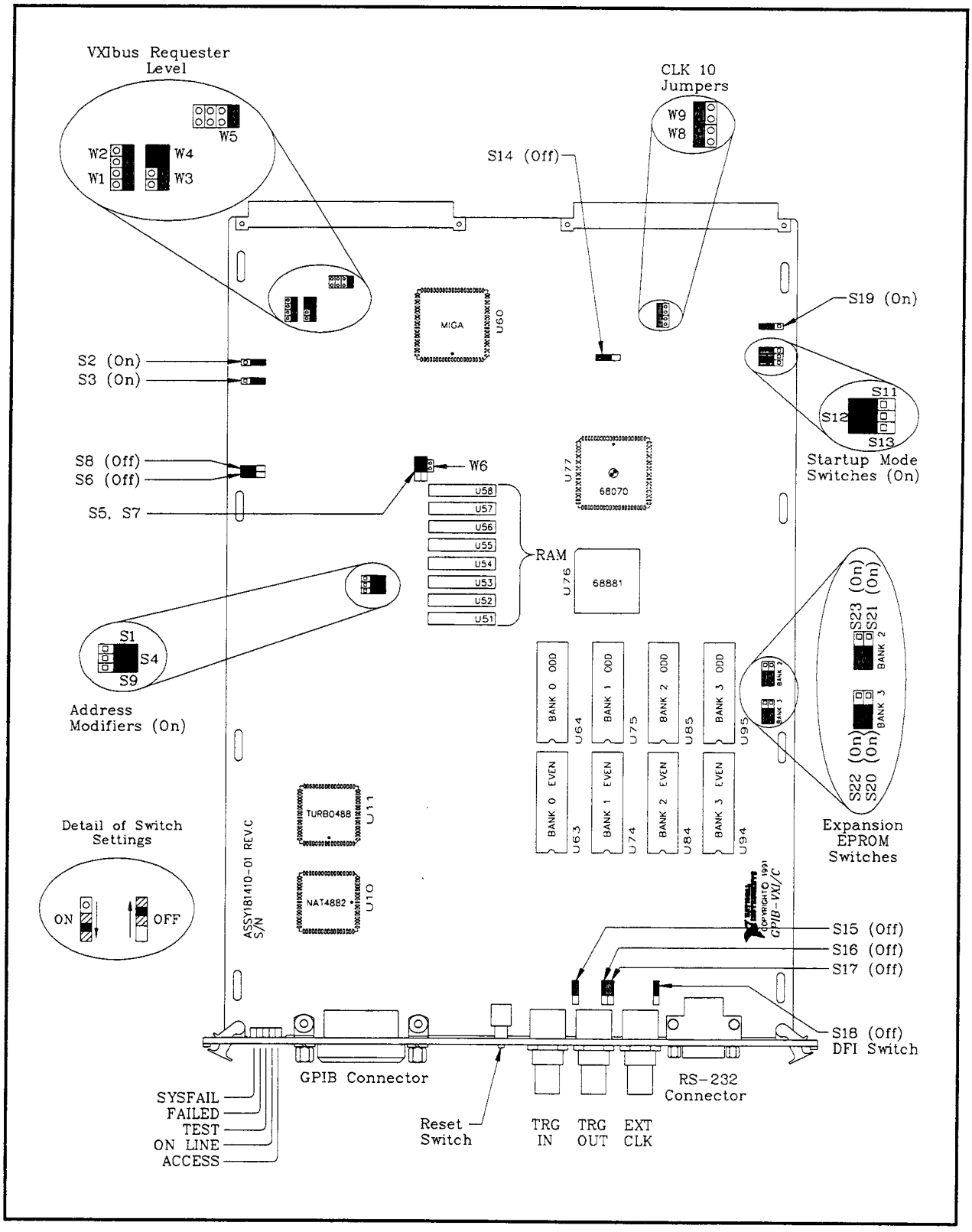

Figure 2-1. GPIB-VXI/C Parts Locator Diagram

Setting the Logical Address, GPIB Primary Address, and Servant Area Size

You can change the logical address, GPIB primary address, and Servant area size by running the nonvolatile memory configuration utility as described in the *Change Configuration Information* section of Chapter 4, *Nonvolatile Configuration*.

Verifying the Installed RAM Size

Up to 4 megabytes of local RAM can be factory-installed on the GPIB-VXI/C. The minimum amount of memory is 512 kilobytes. Table 2-2 lists the RAM configurations and their associated switch settings. You can use this information to verify the board configuration.

Table 2-2. Installed RAM Configuration

Installed Memory Size	Switch S7 Setting	Switch S5 Setting	Jumper W6 Setting
512 kilobytes	OFF	OFF	OFF
1 megabyte	OFF	ON	OFF
2 megabytes	ON	OFF	ON
4 megabytes	ON	ON	ON

Table 2-3 shows the relationship between the amount of installed memory, the local address range occupied by the memory, and the range of VXI A24 addresses accessible by the GPIB-VXI/C as a bus master.

Table 2-3. GPIB-VXI/C CPU Local and A24 Memory Ranges

Installed Memory Size	Installed Memory Local Address Range		Accessible VXI A24 Address Range	
	Start	**End**	**Start**	**End**
512 kilobytes	000000h	07FFFFh	080000h	E7FFFFh
1 megabyte	000000h	0FFFFFh	100000h	E7FFFFh
2 megabytes	000000h	1FFFFFh	200000h	E7FFFFh
4 megabytes	000000h	3FFFFFh	400000h	E7FFFFh

Setting the Shared Memory Size

You can set the amount of installed memory that is shared with the VXIbus by altering the settings of switches S8 and S6. Table 2-4 gives the S8 and S6 switch settings for sharing various portions of RAM with the VXIbus for each possible installed memory configuration.

Table 2-4. Shared Memory Switch Settings

Installed Memory Size	Amount of Installed Memory Shared with VXIbus			
	S6 ON S8 ON	**S6 ON S8 OFF**	**S6 OFF S8 ON**	**S6 OFF S8 OFF**
512 kilobytes	512 kilobytes	256 kilobytes	128 kilobytes	none
1 megabyte	1 megabyte	512 kilobytes	256 kilobytes	none
2 megabytes	2 megabytes	1 megabyte	512 kilobytes	none
4 megabytes	4 megabytes	2 megabytes	1 megabyte	none

Note: The RAM shared with the VXIbus will be the upper portion of the installed memory.

The GPIB-VXI/C Offset Register holds the shared memory VXI A24 base address, as described in the VXIbus specification. The RM automatically configures the Offset Register at startup.

Setting the Reset Operation

The GPIB-VXI/C has three configurable reset parameters. They can be enabled or disabled and are as follows:

- Pushbutton resets backplane (asserts SYSRESET* signal).
- Pushbutton resets GPIB-VXI/C (asserts local reset signal).
- Backplane SYSRESET* signal resets GPIB-VXI/C (SYSRESET* on backplane asserts local reset).

The reset parameters can be altered by the nonvolatile memory configuration as described in the *Change Configuration Information* section of Chapter 4.

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